PMW3901MB-TXQT: Optical Motion Tracking Chip

Product Datasheet

General Description

The PMW3901MB-TXQT is PixArt Imaging's latest optical navigation chip designed with far field optics technology that enables navigation in the air. It is housed in a 28-pin chip-on-board (COB) package that provides X-Y motion information with a wide working range of 80 mm to infinity. It is most suitable for far field application for motion detection.

Key Features

- Wide working range from 80 mm to infinity
- No lens focusing required during lens mounting process
- Power consumption of < 9 mA @ run mode
- 16-bits motion data registers
- Motion detect pin output
- Internal oscillator – no clock input needed

Applications

- Devices that require far field motion detection, e.g Drone
- Indoor and outdoor X-Y positioning especially in GPS denied environment

Key Parameters

Parameter	Value
Supply Voltage (V)	V_{DD}: 1.8 – 2.1 V_{DDIO}: 1.8 – 3.6
Working Range (mm)	80 to infinity
Interface	4-Wire SPI @ 2 MHz
Package Type	28-pin COB Package with Lens Assembly: 6 x 6 x 2.28 mm

Ordering Information

Part Number	Package Type
PMW3901MB-TXQT	28-pin COB Package
LN03-ZSZ	Lens Assembly

RoHS compliant

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1.0 Introduction

1.1 Overview

PMW3901MB-TXQT is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential picture elements and mathematically determining the direction and magnitude of movement. PMW3901MB contains a Picture Element Acquisition System (PEAS), a hard-coded Digital Signal Processing System (DSPS), and a four-wire serial port interface. The picture elements acquired by the PEAS are processed by the DSPS to determine the direction and distance of motion. The DSPS calculates the delta X and delta Y relative displacement. An external microcontroller reads and translates the delta X and delta Y information from PMW3901MB into radio frequency signals before sending them to the host.

Figure 1 below shows the functional block diagram of PMW3901MB. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

This datasheet describes the electrical characteristics, configuration specifications, I/O timings, and provides recommendations for handling PMW3901MB and its lens assembly.

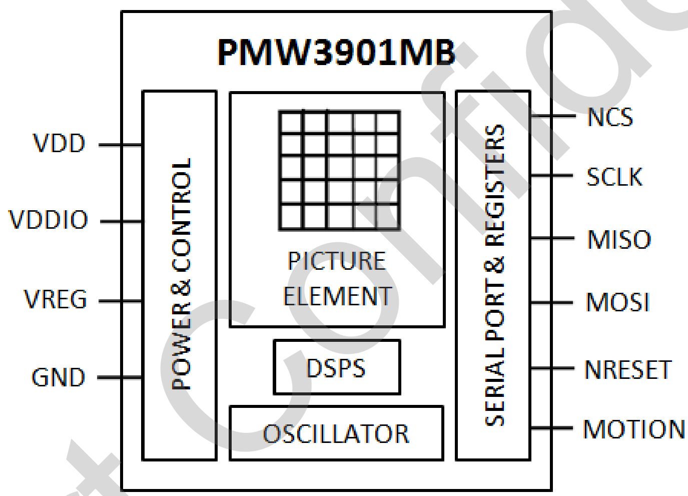


Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
DSPS	Digital Signal Processing System
ESD	Electrostatic Discharge
LED	Light Emitting Diode
IC	Integrated Circuit
I/O	Input / Output
IR	Infrared
MCU	Microcontroller Unit
PCB	Printed Circuit Board

1.3 Signal Description

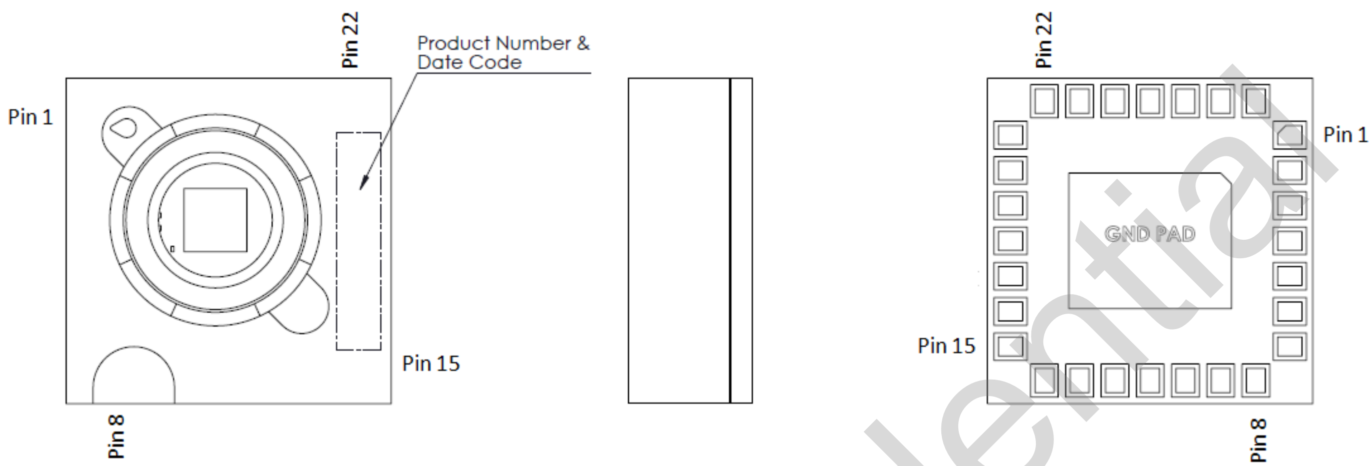


Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
2	VDD	Power	Input power supply
3	VDDIO	Power	I/O reference voltage
4	VREG	Power	Internal voltage output
1	GND	Ground	Ground
21	GND	Ground	Ground
Functional Group:		Control Interface	
16	MOSI	Input	Serial data input
17	SCLK	Input	Serial data clock
18	MISO	Output	Serial data output
19	NCS	Input	Chip select
Functional Group:		Functional I/O	
7	NRESET	Input	Hardware reset (Active low)
15	MOTION	Output	Motion interrupt (Active low)
20	LED_N	Input	External LED control pin (Active low) (Refer **Appendix B** for more details)
Functional Group:		Special Function Pin	
5 - 6	NC	NC	No connection (float)
8 - 14	NC	NC	No connection (float)
22 - 28	NC	NC	No connection (float)
29*	GND PAD	Ground Pad	Bottom of COB package must be connected to circuit ground

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temperature	T_{SOLDER}		260	°C	
Supply Voltage	V_{DD}	-0.5	2.1	V	
	V_{DDIO}	-0.5	3.6	V	
Input Voltage	V_{IN}	-0.5	3.6	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
3. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	1.8	2.0	2.1	V	Including supply noise
	V_{DDIO}	1.8	2.0	3.6	V	$V_{DDIO} \geq V_{DD}$
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to V_{DD} min
Supply Noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	10 kHz – 75 MHz
Serial Port Clock Frequency	f_{SCLK}			2	MHz	50% duty cycle
Working Range	Z	80			mm	
Effective Viewing Angle	V_A		42		°	
Illuminance	Lx	60			lux	Tested under florescent light on crimson carpet, light grey vinyl & light grey cement surfaces.
Speed	S			7.4	rad/s	

Note: PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current	I_{DD_RUN}		9		mA	Average current. No load on MISO, MOTION.
Power Down Current	I_{PD}		12		uA	
Input Low Voltage	V_{IL}			0.3*V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7*V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	uA	V_{in} = V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} - 0.45			V	I_{OUT} = -1mA, MISO, MOTION

Note: All the parameters are tested under operating conditions: V_{DD} = 2.0V, V_{DDIO} = 2.0V, T_A = 25°C.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Motion Delay After Reset	$t_{MOT\text{-}RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	us	From Shutdown mode active to low current
Wake from Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown", also note $t_{MOT\text{-}RST}$.
MISO Rise Time	$t_{r\text{-}MISO}$		50		ns	C_L = 100pF
MISO Fall Time	$t_{f\text{-}MISO}$		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY\text{-}MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold\text{-}MISO}$	200			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold\text{-}MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup\text{-}MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	45			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	45			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	35			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.

NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS\text{-}SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK\text{-}NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK\text{-}NCS}$	35			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS\text{-}MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r\text{-}MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f\text{-}MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150 us and max 20 ms rise time (does not include charging currents for bypass capacitors).
	I_{DDTIO}			70	mA	Max supply current during the supply ramp from 0V to V_{DDIO} with min 150 us and max 20 ms rise time (does not include charging currents for bypass capacitors).

Note: All the parameters are tested under operating conditions: V_{DD} = 2.0V, V_{DDIO} = 2.0V, T_A = 25°C.

3.0 Mechanical Specifications

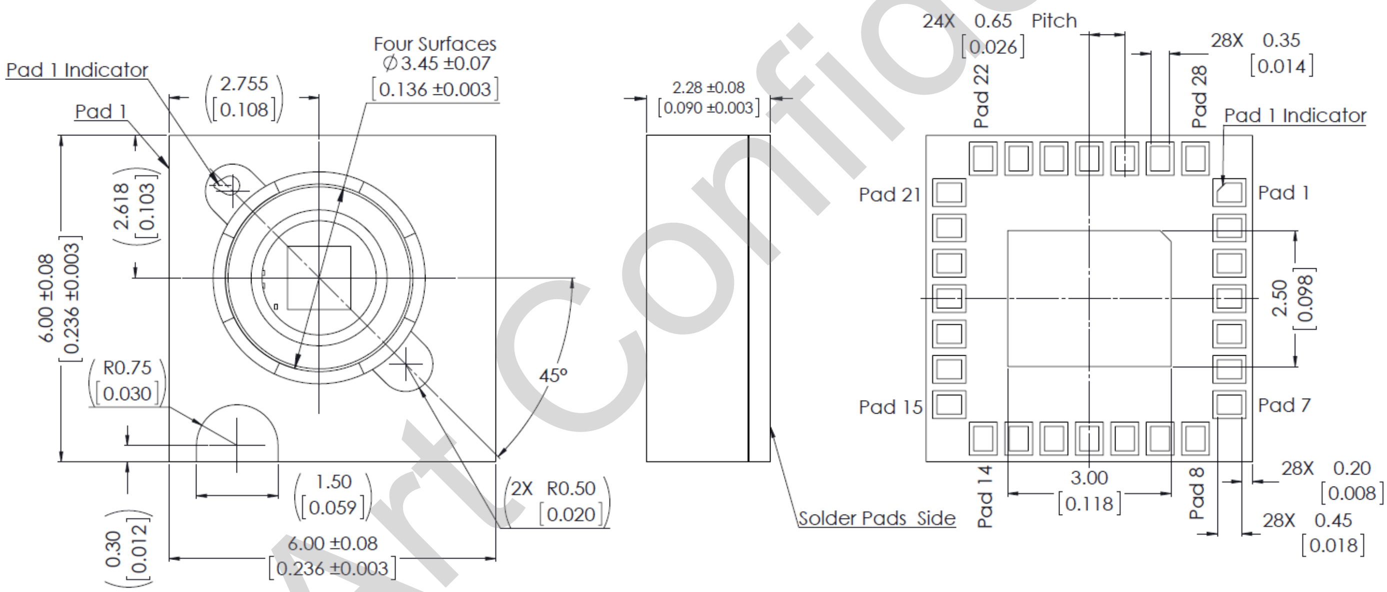
3.1 Package Marking

Refer Figure 2. Pin Configuration for the code marking location on the device package.

Table 6. Code Identification

Code	Marking	Description
Product Number	P3901	Part number label
Lot Code	YWX	Y: Year W: Week X: Reserved as PixArt reference

3.2 Package Outline Drawing



Notes:
1. Dimensions in milimeters [Inches]
2. Coplanarity of pads: 0.08 mm
3. Non-cumulative pad pitch tolerance: ±0.10 mm
4. Maximum flash: ±0.20 mm
5. Dimensional tolerance: ±0.10 mm unless otherwise stated
6. Document number: PMW3901MB-TXQT-G8_004

CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 3. Package Outline Drawing

3.3 Assembly Drawings

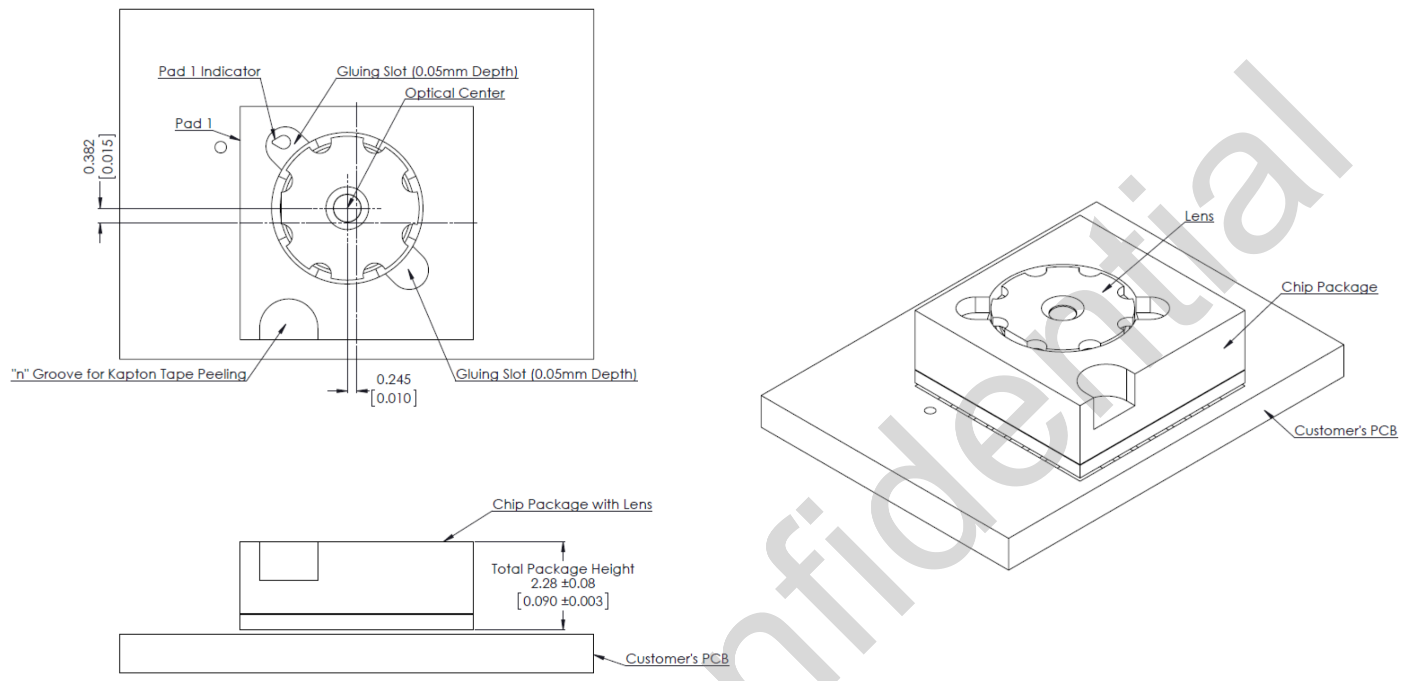


Figure 4. System Assembly View

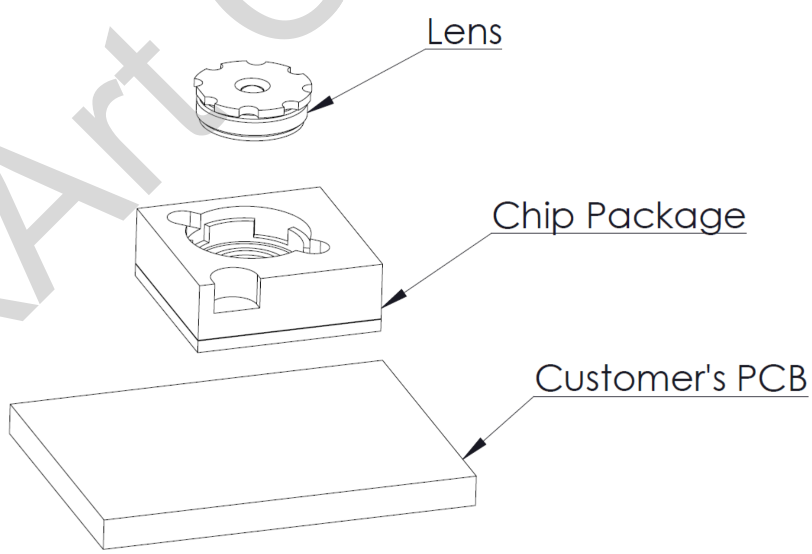
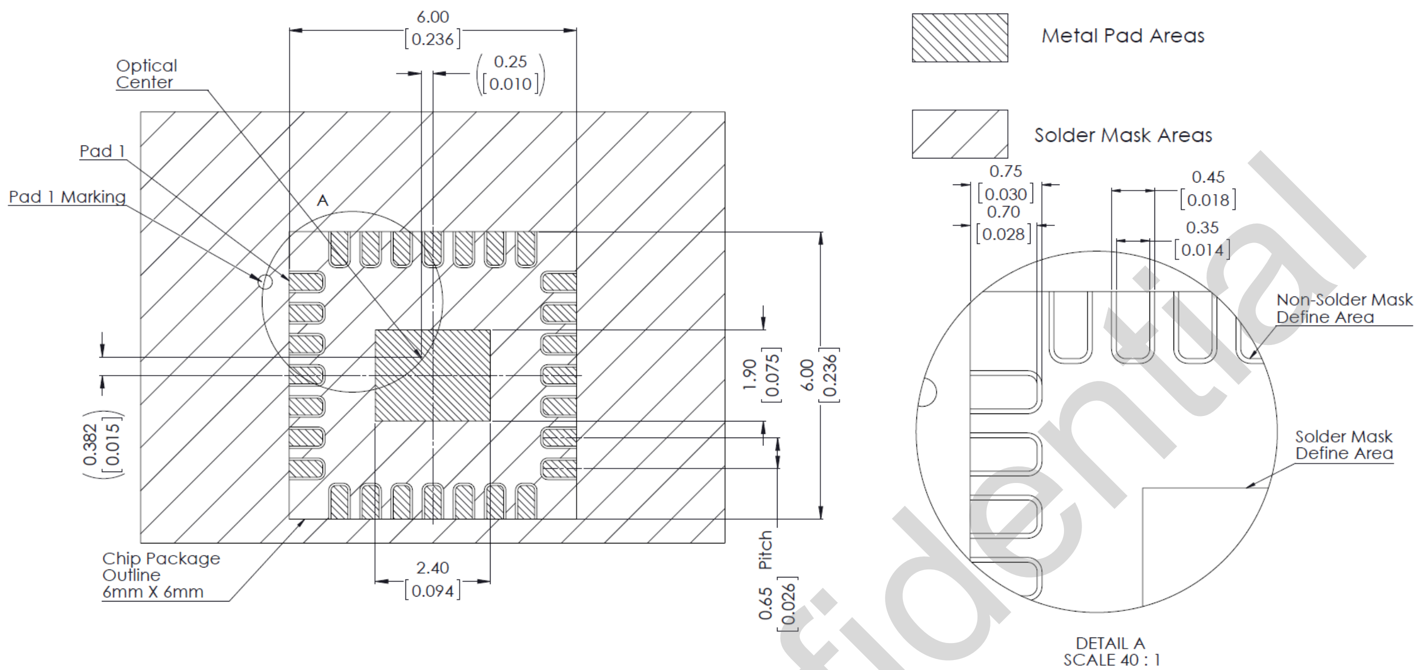


Figure 5. Exploded View of System Assembly



Note: Bottom center pad of COB package must be connected to circuit ground.

Figure 6. Recommended PCB Layout

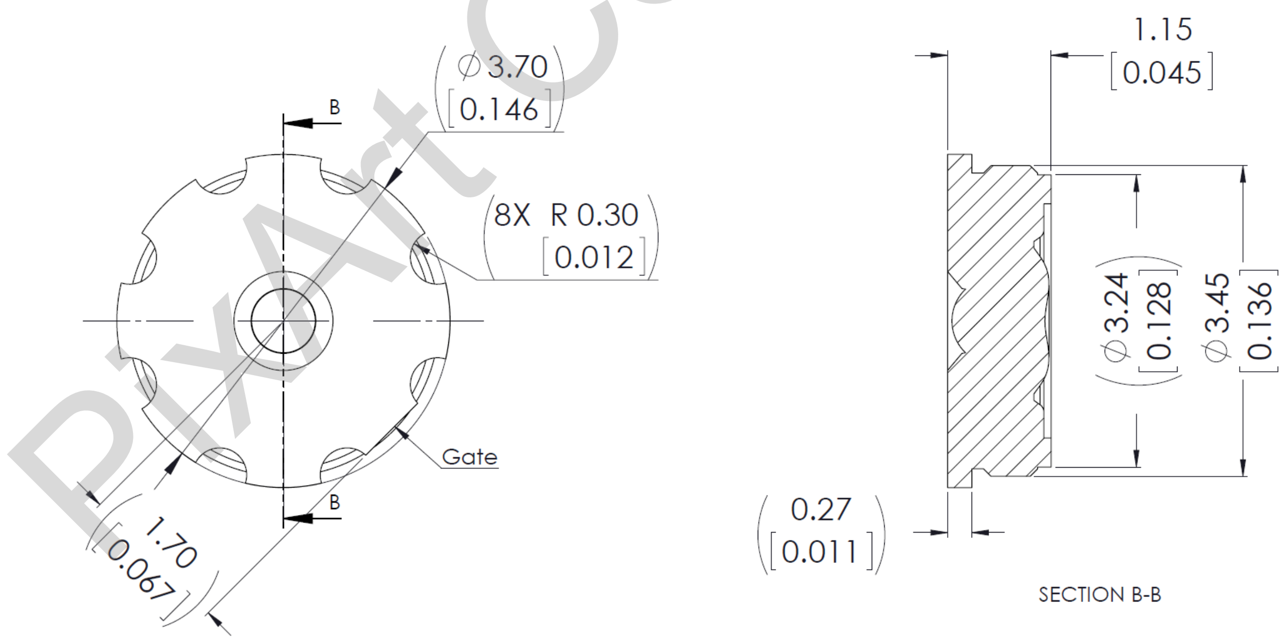
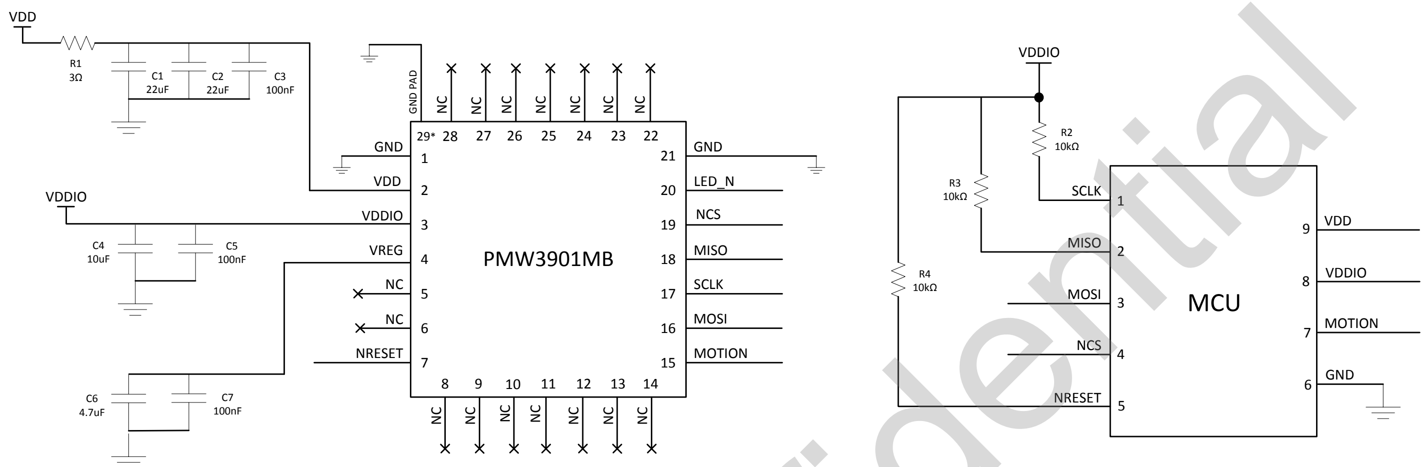


Figure 7. Lens Outline Drawing

4.0 System Level Description

4.1 Reference Schematic



Note:
1. All capacitors must be placed as close as possible to VDD, VDDIO & VREG pins.
2. Ceramic non-polarity capacitors are recommended.

Figure 8. PMW3901MB Reference Schematics

4.2 Assembly Recommendation

- Surface mount PMW3901MB and all other electrical components onto PCB.
- Reflow the entire assembly in a no-wash solder process.
  Note: It is recommended to generate a stencil profile for the reflow process.
- Remove the protective kapton tape on top of the chip's package.
  Note: Care must be taken to keep contamination from entering the aperture.
  Recommendation: Hold the PCB assembly vertically when removing kapton tape.
- Place the PCB assembly horizontally with the top of the chip's package facing up.
- Insert the lens onto the optical aperture (the hole on the chip's package).
- Use a 3.5 mm diameter flat tip jig to press the lens onto the aperture until the top surface of the lens is aligned with the top surface of the chip's package.
  Note: No lens focusing is required.
- Insert the nozzle of glue dispenser vertically inside the gluing slots and dispense glue appropriately.
- Remove the nozzle of glue dispenser and let the glue cure properly.

Note: Refer to PMW3901MB's Application Note for more information and detailed steps of the assembly process.

4.3 Manual re-work of chip assembly

If there is a need to re-work the chip assembly by de-soldering and re-soldering the chip onto PCB, it is advised to do so before applying glue onto the lens' gluing slots. Please note below precautions for re-work of chip assembly:

- Remove lens from the optical aperture by peeling the lens from the gluing slot using a tweezer.
  Note: It is important to remove the lens as it will melt under the soldering heat.
- Place kapton tape across the top of the package to keep contamination from entering the aperture.
- Perform de-soldering & soldering activities as needed.
- Remove kapton tape and insert the lens as outlined in the above section.

5.0 Power States & Sequence

5.1 Power-Up Sequence

Although PMW3901MB performs an internal power up self-reset, it is still recommended that the Power_Up_Reset register is written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDDIO first and followed by VDD, with a delay of no more than 100ms in between each supply. Ensure all supplies are stable.
2. Wait for at least 40 ms.
3. Drive NCS high, and then low to reset the SPI port.
4. Write 0x5A to Power_Up_Reset register (or alternatively, toggle the NRESET pin).
5. Wait for at least 1 ms.
6. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion pin state.
7. Refer Section **8.2 Performance Optimization Registers** to configure the needed registers in order to achieve optimum performance of the chip.

The table below shows the state of the various pins during power-up and reset.

Table 7. State of Signal Pins during Power-Up & Reset

State of Signal Pins after VDD is Valid		
Pin	**During Reset**	**After Reset**
NRESET	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

Note: The NRESET pin can be used to perform a full chip reset. When asserted, it performs the same function as the Power_Up_Reset register. The NRESET pin needs to be asserted (held to logic 0) for at least 100 ns. The NRESET pin cannot be left floating or unconnected.

5.2 Power-Down Sequence

PMW3901MB can be set to Shutdown mode by writing to Shutdown register. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5A to register 0x3A). Other ICs on the same SPI bus can be accessed, as long as the chip's NCS pin is not asserted.

To de-assert Shutdown mode:

1. Drive NCS high, and then low to reset the SPI port.
2. Write 0x5A to Power_Up_Reset register (or alternatively, toggle the NRESET pin).
3. Wait for at least 1 ms.
4. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion pin state.
5. Refer Section **8.2 Performance Optimization Registers** to configure the needed registers in order to achieve optimum performance of the chip.

The table below shows the state of various pins during shutdown.

Table 8. State of Signal Pins during Shutdown.

Pin	Status during Shutdown Mode
NRESET	High
NCS	High [1]
MISO	Hi-Z [2]
SCLK	Ignore if NCS = 1 [3]
MOSI	Ignore if NCS = 1 [4]
MOTION	Output High

Notes:

1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Shutdown unless powering up the chip. It must be held to 0 (low) if the chip is to be re-powered up from shutdown (writing 0x5A to register 0x3A).
2. MISO should be either pull up or down during shutdown.
3. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).
4. MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5A to register 0x3A).

6.0 Serial Port Interface Communication

6.1 Signal Description

The synchronous serial port is used to set and read parameters in PMW3901MB, and to read out the motion information.

The port is a four wire port. The host microcontroller always initiates communication; PMW3901MB never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port are:

Pin	Description
SCLK	Clock input, generated by the master (microcontroller).
MOSI	Input data (Master Out / Slave In).
MISO	Output data (Master In / Slave Out).
NCS	Chip select input (active low). NCS needs to be low to activate the serial port; otherwise MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

6.2 Motion Pin Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is non-zero data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit (by reading Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers, or writing to the Motion register) will put the motion pin high.

6.3 Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction.

To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state.

In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

6.4 Write Operation

Write operation, defined as data going from the micro-controller to PMW3901MB, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. PMW3901MB reads MOSI on rising edges of SCLK.

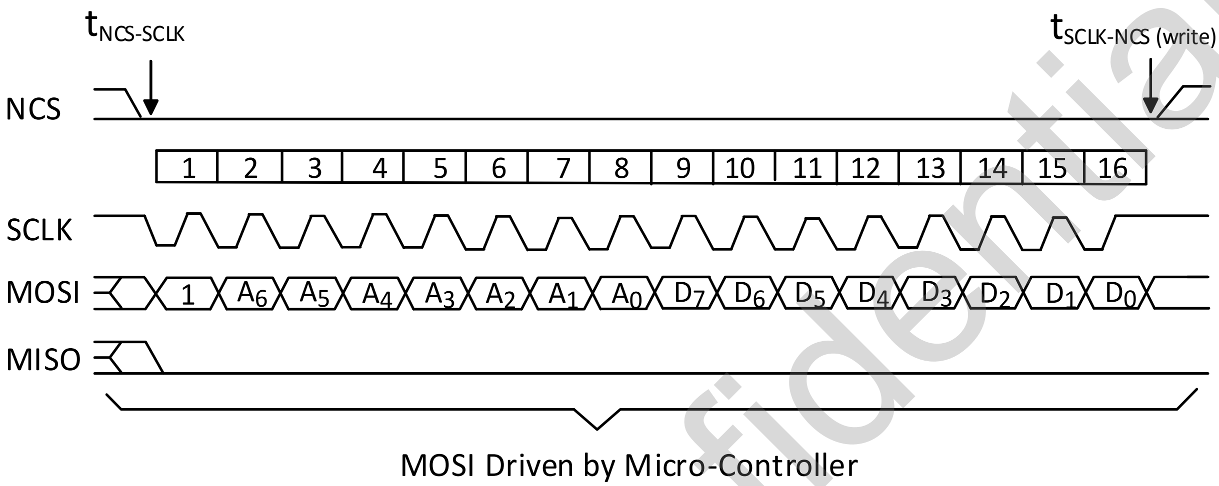


Figure 9. Write Operation

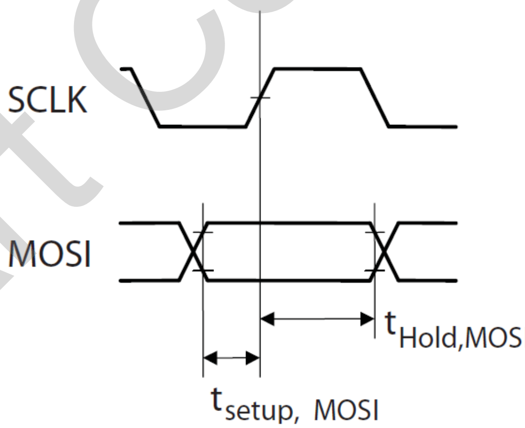


Figure 10. MOSI Set-up and Hold Time

6.5 Read Operation

A read operation, defined as data going from PMW3901MB to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by PMW3901MB over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

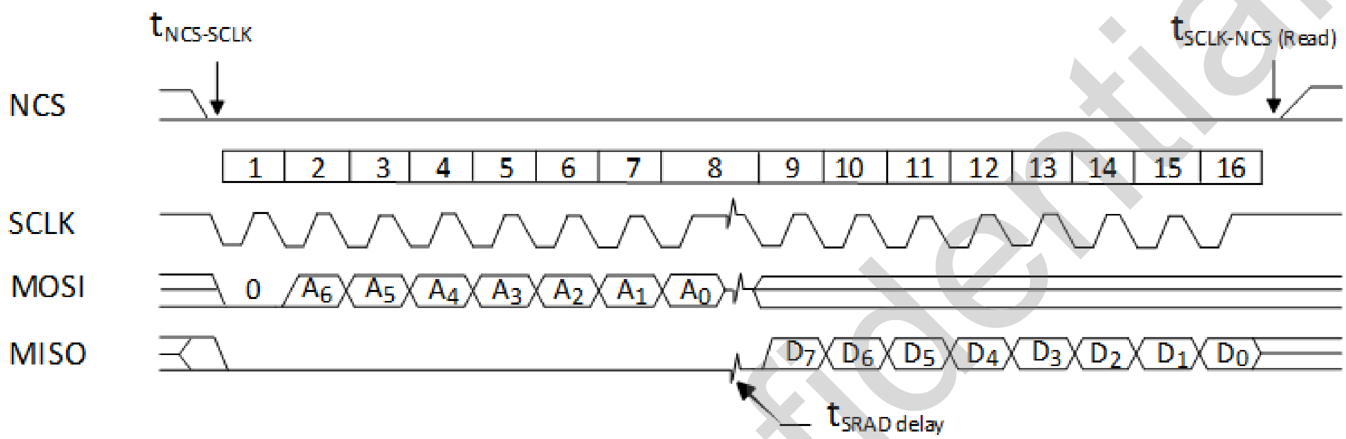


Figure 11. Read Operation

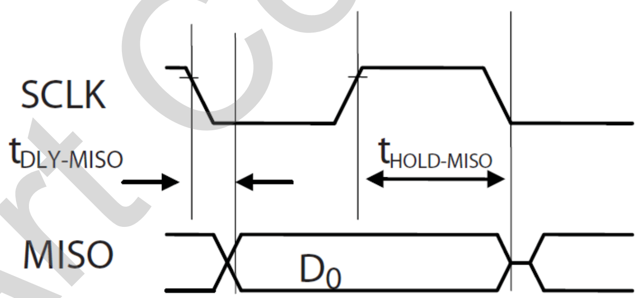


Figure 12. MISO Delay and Hold Time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of PMW3901MB. Since the falling edge of SCLK is actually the start of the next read or write command, PMW3901MB will hold the state of data on MISO until the falling edge of SCLK.

6.6 Required Timing between Read and Write Commands (t_{SXX})

There are minimum timing requirements between read and write commands on the serial port.

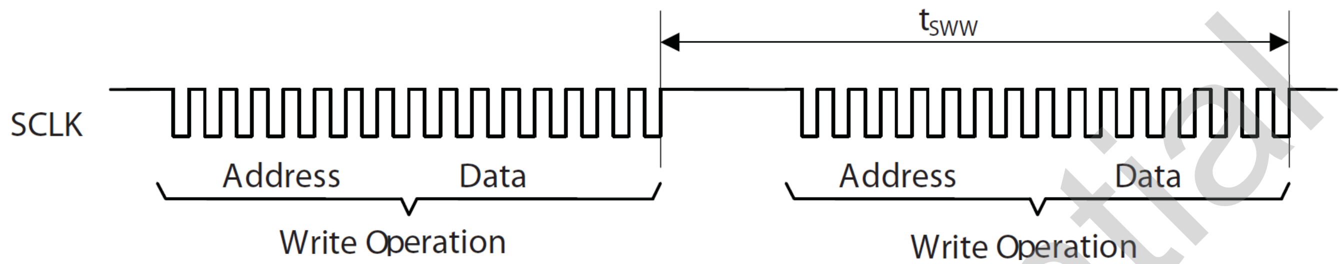


Figure 13. Timing between two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{SWW} delay, then the first write command may not complete correctly.

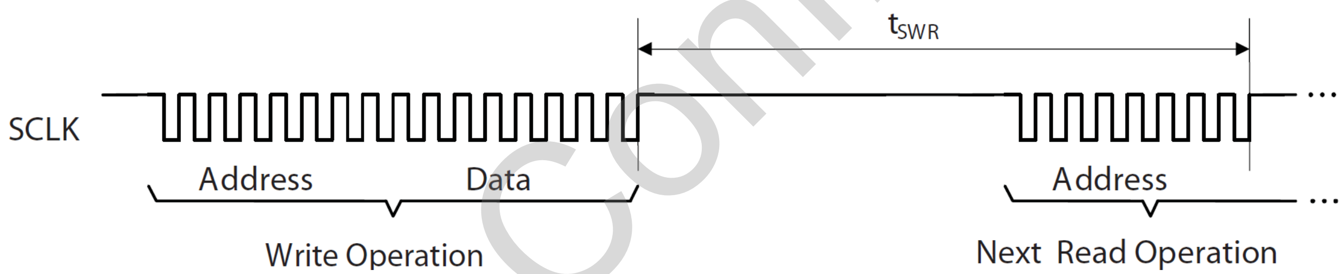


Figure 14. Timing between Write and Read commands

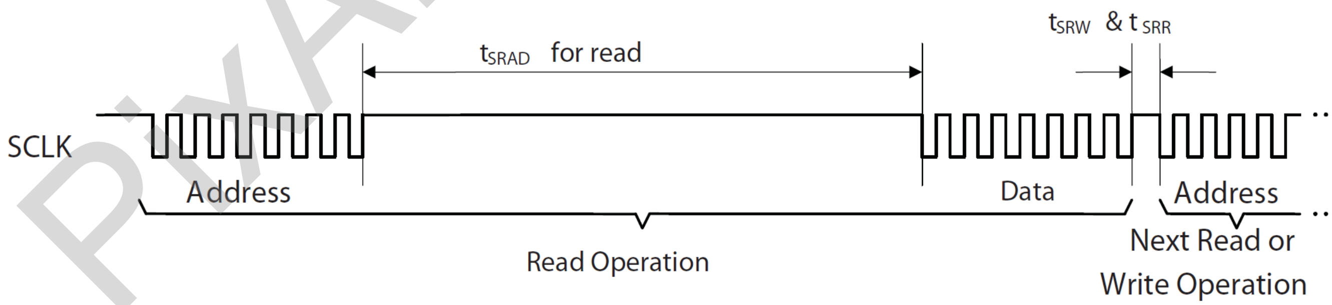


Figure 15. Timing between Read and either Write or subsequent Read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not complete correctly. During a read operation, SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that PMW3901MB has time to prepare the requested data.

7.0 Operation

7.1 Burst Mode

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for Motion Read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

7.2 Motion Read

Reading the Motion_Burst register activates Burst Mode. PMW3901MB will respond with the following motion burst report in order.

Motion burst report:

BYTE[00] = Motion

BYTE[01] = Observation

BYTE[02] = Delta_X_L

BYTE[03] = Delta_X_H

BYTE[04] = Delta_Y_L

BYTE[05] = Delta_Y_H

BYTE[06] = SQUAL

BYTE[07] = RawData_Sum

BYTE[08] = Maximum_RawData

BYTE[09] = Minimum_RawData

BYTE[10] = Shutter_Upper

BYTE[11] = Shutter_Lower

After sending the register address, the microcontroller must wait for t_{SRAD}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Procedure to start motion burst:

1. Lower NCS signal, and wait for $t_{NCS\text{-}SCLK}$ delay.
2. Send Motion_Burst address (0x16). After sending this address, MOSI should be held either high or low until the burst transmission is complete (MOSI should not be toggling during subsequent SCLK cycles).
3. Wait for t_{SRAD}.
4. Start reading SPI Data continuously up to 12 bytes. Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. Check SQUAL & Shutter_Upper values. To suppress false motion reports, discard Delta_X and Delta Y values if the SQUAL value < 0x19 and Shutter_Upper = 0x1F.
6. To read new motion burst data, repeat from step 1.

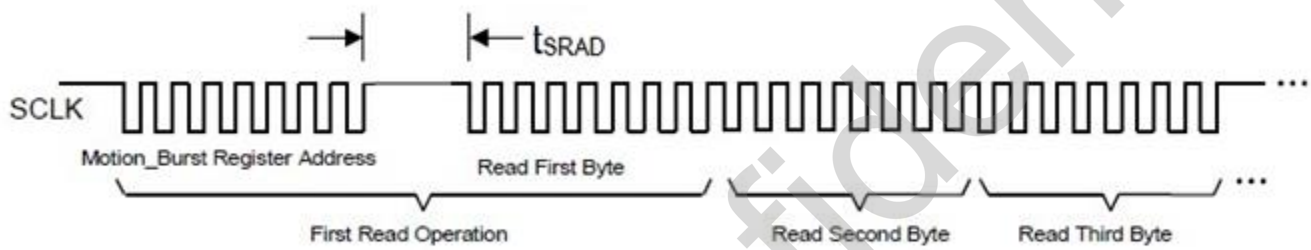


Figure 16. Motion Read Timing

7.3 Frame Capture

Frame Capture is the method to download the full array of raw data values using register read operation. This mode disables navigation and no other SPI activity is allowed during this period. A hardware reset is required to restore navigation.

Power-Up sequence should have been completed before performing Frame Capture. Frame Capture procedure is outlined below:

1. To enter Frame Capture mode, perform the below register writes in sequence:

Address	Value
0x7F	0x07
0x41	0x1D
0x4C	0x00
0x7F	0x08
0x6A	0x38
0x7F	0x00
0x55	0x04
0x40	0x80
0x4D	0x11

2. Write value 0x00 to register 0x70, and then write value 0xFF to register 0x58.

3. Poll RawData_Grab_Status register until both bits 6 & 7 are set before proceeding to the next step.

4. Read raw data from RawData_Grab register. Each raw data consists of 8-bits and is constructed as described below:

Register Name	RawData_Grab							
				Address	0x58			
Access	R/W			Reset Value	0x00			
Bit	7	6	5	4	3	2	1	0
Field	RDG_7	RDG_6	RDG_5	RDG_4	RDG_3	RDG_2	RDG_1	RDG_0
Description	This register is used to read out the full array of raw data values. PMW3901MB needs to be held stationary for the duration of grabbing raw data until the full array is completely read out, as the information is read out one data at a time. This process is initialized by a single write of any value to this register. Reading this register will unload 8-bits raw data at a time, toggling between upper 6-bits and lower 2-bits.							

Field	Access	Reset	Value	Description
RDG[5:0]	R/W	0		Raw data values
RDG[7:6]	R/W	0		Flag to indicate which bits of raw data is being grabbed
			00	Invalid (raw data not available). Continue to poll RawData_Grab register.
			01	Raw data is valid and available. Upper 6-bits raw data are held in RDG[5:0].
			10	Raw data is valid and available. Lower 2-bits raw data are held in RDG[3:2]. Reading of lower 2-bits always follow the read of upper 6-bits of raw data.
			11	Invalid (raw data not available). Continue to poll RawData_Grab register.

5. Construct each raw data by assigning upper 6-bits values from RDG[5:0] as RawData[7:2] and assigning lower 2-bits values from RDG[3:2] as RawData[1:0].

6. Continue Steps (4) and (5) until all 1225 raw data are read.

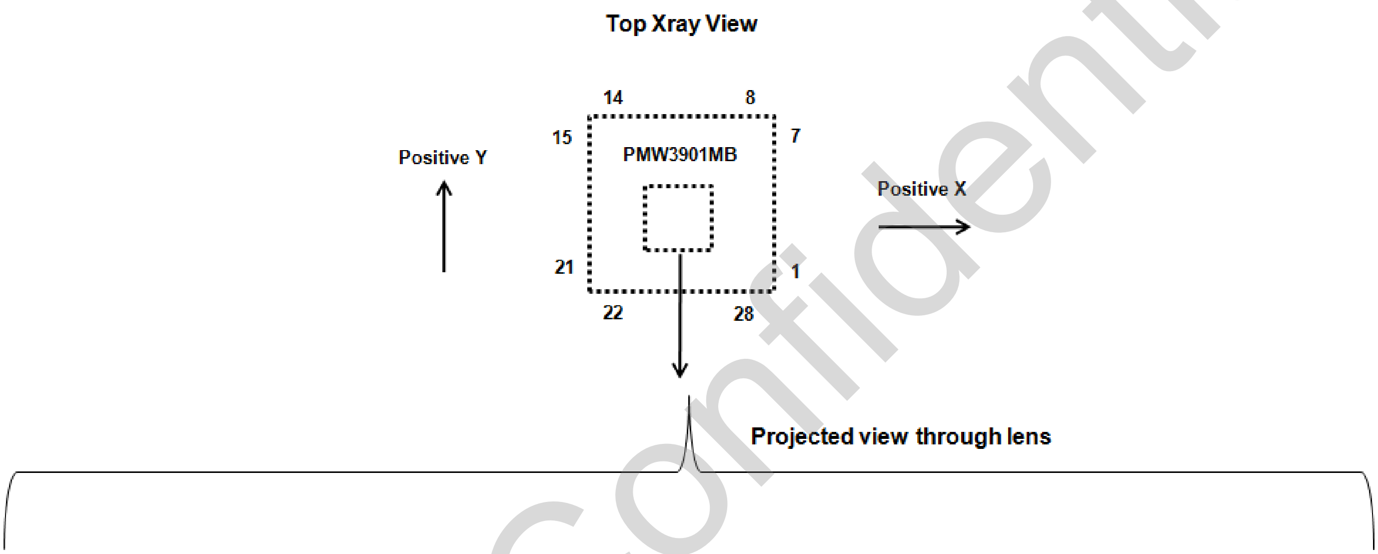
7. To capture another frame, repeat Steps (2) to (6).

8. To exit Frame Capture mode, perform the below register writes in sequence:

Address	Value
0x7F	0x00
0x4D	0x11
0x40	0x80
0x55	0x80
0x7F	0x08
0x6A	0x18

Address	Value
0x7F	0x07
0x41	0x0D
0x4C	0x80
0x7F	0x00

Note: Manual reset is needed after frame capture to restore navigation.



First output

34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	▪	▪	12	11	10	9	8	7	6	5	4	3	2	1	0
69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	▪	▪	47	46	45	44	43	42	41	40	39	38	37	36	35
104	103	102	101	100	99	98	97	96	95	94	93	92	91	90	▪	▪	82	81	80	79	78	77	76	75	74	73	72	71	70
▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
1154	1153	1152	1151	1150	1149	1148	1147	1146	1145	1144	1143	1142	1141	1140	▪	▪	1132	1131	1130	1129	1128	1127	1126	1125	1124	1123	1122	1121	1120
1189	1188	1187	1186	1185	1184	1183	1182	1181	1180	1179	1178	1177	1176	1175	▪	▪	1167	1166	1165	1164	1163	1162	1161	1160	1159	1158	1157	1156	1155
1224	1223	1222	1221	1220	1219	1218	1217	1216	1215	1214	1213	1212	1211	1210	▪	▪	1202	1201	1200	1199	1198	1197	1196	1195	1194	1193	1192	1191	1190

Last output

Figure 17. Raw Data Map

8.0 Registers

8.1 Registers List

PMW3901MB registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 9. Register List

Address	Register Name	Access	Reset	Address	Register Name	Access	Reset
0x00	Product_ID	RO	0x49	0x0A	Minimum_RawData	RO	0x00
0x01	Revision_ID	RO	0x00	0x0B	Shutter_Lower	RO	0x00
0x02	Motion	R/W	0x00	0x0C	Shutter_Upper	RO	0x00
0x03	Delta_X_L	RO	0x00	0x15	Observation	R/W	0x00
0x04	Delta_X_H	RO	0x00	0x16	Motion_Burst	RO	0x00
0x05	Delta_Y_L	RO	0x00	0x3A	Power_Up_Reset	WO	N/A
0x06	Delta_Y_H	RO	0x00	0x3B	Shutdown	WO	N/A
0x07	Squal	RO	0x00	0x58	RawData_Grab	R/W	0x00
0x08	RawData_Sum	RO	0x00	0x59	RawData_Grab_Status	RO	0x00
0x09	Maximum_RawData	RO	0x00	0x5F	Inverse_Product_ID	RO	0xB6

8.2 Performance Optimization Registers

Upon power-up of PMW3901MB, there are a number of registers to configure in order to achieve optimum performance of the chip. These registers are PixArt proprietary information, thus no additional information is provided in this datasheet with regards to these register's descriptions. These registers should be written or read in sequence as outlined below:

Table 10. Performance Optimization Registers

Function	Address	Value	Remarks
Write	0x7F	0x00	
Write	0x55	0x01	
Write	0x50	0x07	
Write	0x7F	0x0E	
Write	0x43	0x10	If value 0x08 is not read back, write register 0x43 with value 0x10 and read register 0x47 again. Repeat this for a total of 3 trials. If unsuccessful, exit the routine. Power cycle PMW3901MB and re-attempt the registers' configuration.
Read	0x47	0x08	
Read	0x67	Bit 7 set	Write register 0x48 with value 0x04
		Bit 7 not set	Write register 0x48 with value 0x02
Write	0x7F	0x00	
Write	0x51	0x7B	
Write	0x50	0x00	
Write	0x55	0x00	
Write	0x7F	0x0E	
Read	0x73	Not 0x00	*Skip the next segment with rows highlighted with asterisk*

Read *Read *Read *Write *Write *Write *Write *Write *Write	0x73 0x70 0x71 0x7F 0x61 0x51 0x7F 0x70 0x71	0x00 "C1" "C2" 0x00 0xAD 0x70 0x0E "C1" "C2"	Proceed with the next segment with rows highlighted with asterisk* Assign C1 as the value read back from register 0x70 *If C1 ≤ 28, then C1 = C1 + 14* *If C1 > 28, then C1 = C1 + 11* ** C1 should be capped to a maximum value of 0x3F* Assign C2 as the value read back from register 0x71 *C2 = (C2 x 45) / 100* C1 value as calculated above C2 value as calculated above
Write	0x7F	0x00	
Write	0x61	0xAD	
Write	0x7F	0x03	
Write	0x40	0x00	
Write	0x7F	0x05	
Write	0x41	0xB3	
Write	0x43	0xF1	
Write	0x45	0x14	
Write	0x5B	0x32	
Write	0x5F	0x34	
Write	0x7B	0x08	
Write	0x7F	0x06	
Write	0x44	0x1B	
Write	0x40	0xBF	
Write	0x4E	0x3F	
Write	0x7F	0x08	
Write	0x65	0x20	
Write	0x6A	0x18	
Write	0x7F	0x09	
Write	0x4F	0xAF	
Write	0x5F	0x40	
Write	0x48	0x80	
Write	0x49	0x80	
Write	0x57	0x77	
Write	0x60	0x78	
Write	0x61	0x78	
Write	0x62	0x08	

Write	0x63	0x50	
Write	0x7F	0x0A	
Write	0x45	0x60	
Write	0x7F	0x00	
Write	0x4D	0x11	
Write	0x55	0x80	
Write	0x74	0x1F	
Write	0x75	0x1F	
Write	0x4A	0x78	
Write	0x4B	0x78	
Write	0x44	0x08	
Write	0x45	0x50	
Write	0x64	0xFF	
Write	0x65	0x1F	
Write	0x7F	0x14	
Write	0x65	0x67	
Write	0x66	0x08	
Write	0x63	0x70	
Write	0x7F	0x15	
Write	0x48	0x48	
Write	0x7F	0x07	
Write	0x41	0x0D	
Write	0x43	0x14	
Write	0x4B	0x0E	
Write	0x45	0x0F	
Write	0x44	0x42	
Write	0x4C	0x80	
Write	0x7F	0x10	
Write	0x5B	0x02	
Write	0x7F	0x07	
Write	0x40	0x41	
Write	0x70	0x00	

Delay 10 ms before resuming the below register writes:

Function	Address	Value
Write	0x32	0x44
Write	0x7F	0x07

Function	Address	Value
Write	0x40	0x40
Write	0x7F	0x06
Write	0x62	0xF0
Write	0x63	0x00
Write	0x7F	0x0D
Write	0x48	0xC0
Write	0x6F	0xD5
Write	0x7F	0x00
Write	0x5B	0xA0
Write	0x4E	0xA8
Write	0x5A	0x50
Write	0x40	0x80

8.3 Register Description

8.3.1 Product ID

Table 11. Product ID Related Registers

Usage	Register Addresses
Product identification	0x00, 0x01, 0x5F

Register Name	Product_ID						
			Address		0x00		
Access	RO		Reset Value		0x49		
Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0
Description	This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional.							

Register Name	Revision_ID							
				Address		0x01		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0
Description	This register contains the current IC revision. It is subject to change when new IC versions are released.							

Register Name	Inverse_Product_ID							
				Address		0x5F		
Access	RO			Reset Value		0xB6		
Bit	7	6	5	4	3	2	1	0
Field	$IPID_7$	$IPID_6$	$IPID_5$	$IPID_4$	$IPID_3$	$IPID_2$	$IPID_1$	$IPID_0$
Description	This value is the inverse of the Product_ID. It is used to test the SPI port hardware.							

8.3.2 Reset and Shutdown Related Registers

Table 12. Reset and Shutdown Related Registers

Usage	Register Addresses
Reset / shutting down the chip	0x3A, 0x3B

Register Name	Power_Up_Reset							
				Address		0x3A		
Access	WO			Reset Value		N/A		
Bit	7	6	5	4	3	2	1	0
Field	PUR_7	PUR_6	PUR_5	PUR_4	PUR_3	PUR_2	PUR_1	PUR_0
Description	Write 0x5A to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode and to restore normal operation after Frame Capture.							

Register Name	Shutdown							
				Address		0x3B		
Access	WO			Reset Value		N/A		
Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
Description	Write 0xB6 to this register to set the chip to shutdown mode. Refer Section **5.2 Power-Down Sequence** for more details and on the recovery procedure.							

8.3.3 Motion Related Registers

Table 13. Motion Related Registers

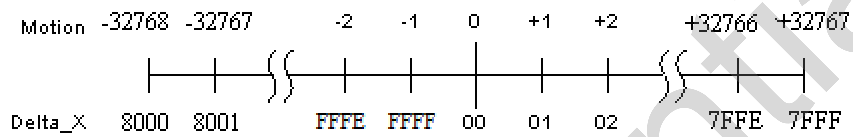
Usage	Register Addresses
Motion report status, accessing & logging data output	0x02, 0x03, 0x04, 0x05, 0x06, 0x16

<table>
<tr><th>Register Name</th><th colspan="8">Motion</th></tr>
<tr><td></td><td colspan="3"></td><td colspan="2">Address</td><td colspan="3">0x02</td></tr>
<tr><td>Access</td><td colspan="3">R/W</td><td colspan="2">Reset Value</td><td colspan="3">0x00</td></tr>
<tr><td rowspan="2">Bit
Field</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MOT_7</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Description</td><td colspan="8">This register allows user to determine if motion has occurred since the last time it was read. The procedure to read the motion registers is as follows:
1. Read the Motion register. This will freeze the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values.
2. If Bit 7 is set, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL and Shutter_Upper registers should be read in sequence to get the accumulated motion.
Note: If Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost.
3. To suppress false motion reports, discard Delta_X and Delta Y values if the SQUAL value < 0x19 and Shutter_Upper = 0x1F.
4. To read a new set of motion data (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H), repeat from Step (1).

Note: Writing anything to this register clears the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers.</td></tr>
</table>

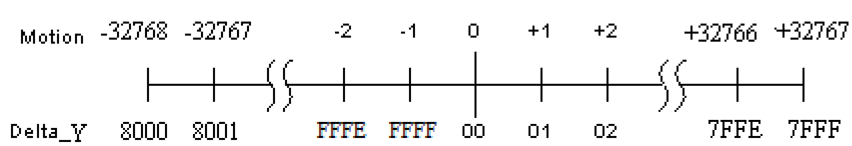
<table>
<tr><th>Field</th><th>Access</th><th>Reset</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="3">MOT_7</td><td rowspan="3">R/W</td><td rowspan="3">0</td><td></td><td>Motion since last report</td></tr>
<tr><td>0</td><td>No motion</td></tr>
<tr><td>1</td><td>Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers.</td></tr>
</table>

Register Name	Delta_X_L							
				Address		0x03		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Description	X movement counts since last report. Absolute value is determined by resolution. Reading it clears the register.							



Register Name	Delta_X_H							
				Address		0x04		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8
Description	Delta_X_H must be read after Delta_X_L to have the full motion data. Reading it clears the register. Note: It is recommended that registers 0x02, 0x03, 0x04, 0x05 and 0x06 be read sequentially.							

Register Name	Delta_Y_L							
				Address		0x05		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
Description	Y movement counts since last report. Absolute value is determined by resolution. Reading it clears the register.							



Register Name	Delta_Y_H							
				Address	0x06			
Access	RO			Reset Value	0x00			
Bit	7	6	5	4	3	2	1	0
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8
Description	Delta_Y_H must be read after Delta_Y_L to have the full motion data. Reading it clears the register. Note: It is recommended that registers 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.							

Register Name	Motion_Burst							
				Address	0x16			
Access	RO			Reset Value	0x00			
Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0
Description	The Motion_Burst register is used for high-speed access of up to 12 register bytes. See **Section 7.2 Motion Read** for use details.							

8.3.4 Operational Check Related Registers

Table 14. Operational Check Related Registers

Usage	Register Addresses
Read only registers - Provide information related to chip's performance.	0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C

Register Name	SQUAL						
			Address		0x07		
Access	RO		Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0
Description	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features: *Number of Features = SQUAL Register Value * 4* The maximum SQUAL register value is 0xFF. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. SQUAL values are only valid in run mode.							

Register Name	RawData_Sum							
			Address		0x08			
Access	RO		Reset Value		0x00			
Bit	7	6	5	4	3	2	1	0
Field	RDS_7	RDS_6	RDS_5	RDS_4	RDS_3	RDS_2	RDS_1	RDS_0
Description	This register is used to find the average raw data value. To find the average raw data value, use the formula below: *Average Raw Data = (Register Value * 2048) / 1225* The maximum register value is 0x98. The minimum register value is 0. The RawData_Sum value can change every frame.							

Register Name	Maximum_RawData							
				Address		0x09		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MRD_7	MRD_6	MRD_5	MRD_4	MRD_3	MRD_2	MRD_1	MRD_0
Description	Maximum raw data value in current frame. Minimum value = 0, maximum value = 255. The maximum raw data value can change every frame.							

Register Name	Minimum_RawData							
				Address		0x0A		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	$MinRD_7$	$MinRD_6$	$MinRD_5$	$MinRD_4$	$MinRD_3$	$MinRD_2$	$MinRD_1$	$MinRD_0$
Description	Minimum raw data value in current frame. Minimum value = 0, maximum value = 255. The minimum raw data value can change every frame.							

Register Name	Shutter_Lower							
				Address		0x0B		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
Description	Lower byte of the 13-bit Shutter register.							

Register Name	Shutter_Upper							
				Address		0x0C		
Access	RO			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	S_{12}	S_{11}	S_{10}	S_9	S_8
Description	Upper 5-bit of the 13-bit Shutter register. Unit is clock cycles of the internal oscillator. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average raw data values within normal operating range. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode.							

8.3.5 Troubleshooting Related Registers

Table 15. Troubleshooting Related Registers

Usage	Register Addresses
Dumping datalogs / information	0x15, 0x58, 0x59

Register Name	Observation							
				Address		0x15		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	OB$_5$	OB$_4$	OB$_3$	OB$_2$	OB$_1$	OB$_0$
Description	User must clear the register by writing 0x00, wait for 15 ms, and read the register. The active processes OB[5:0] will have set their corresponding bits. The read back value should be 0xBF. This register may be used as part of recovery scheme to detect a problem caused by EFT/B or ESD by monitoring OB[5:0].							

Register Name	RawData_Grab							
				Address		0x58		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RDG$_7$	RDG$_6$	RDG$_5$	RDG$_4$	RDG$_3$	RDG$_2$	RDG$_1$	RDG$_0$
Description	This register is used to read out the full array of raw data values. PMW3901MB needs to be held stationary for the duration of grabbing raw data until the full array is completely read out, as the information is read out one data at a time. This process is initialized by a single write of any value to this register. Reading this register will unload 8-bits raw data at a time, toggling between upper 6-bits and lower 2-bits. Refer **Section 7.3 Frame Capture** for more details.							

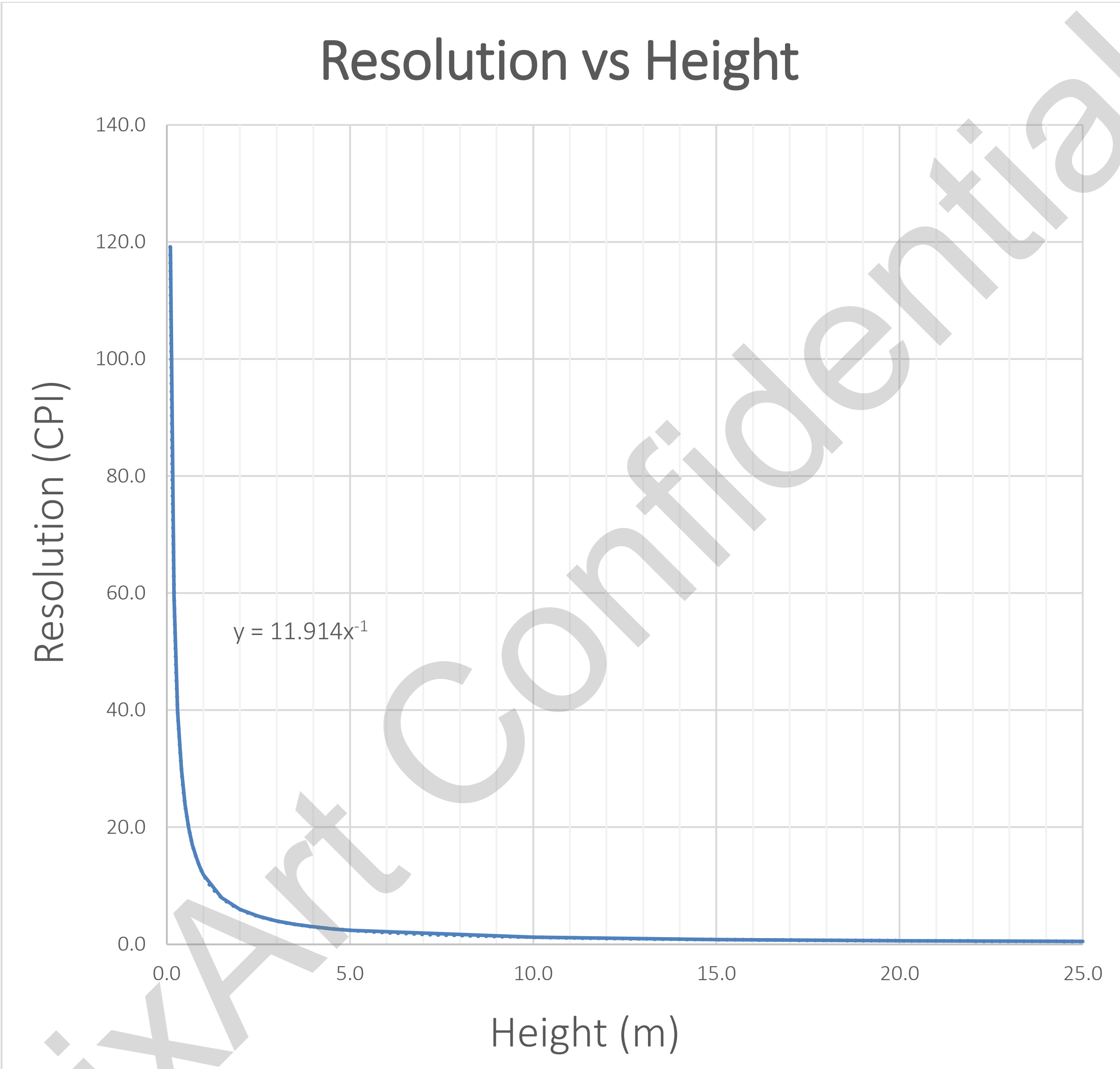
Field	Access	Reset	Value	Description
RDG[5:0]	R/W	0		Raw data values
RDG[7:6]	R/W	0		Flag to indicate which bits of raw data is being grabbed
			00	Invalid (raw data not available).
			01	Raw data is valid and available. Upper 6-bits raw data are held in RDG[5:0].
			10	Raw data is valid and available. Lower 2-bits raw data are held in RDG[3:2].
			11	Invalid (raw data not available).

Register Name	RawData_Grab_Status						
			Address		0x59		
Access	RO		Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	$RDGS_7$	$RDGS_6$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	This register provides status of raw data grab process. Refer **Section 7.3 Frame Capture** for more details.							

Field	Access	Reset	Value	Description
$RDGS_6$	RO	0	0	Raw data is not from location 0,0
			1	Raw data is from location 0,0
$RDGS_7$	RO	0	0	Raw data grab is not valid
			1	Raw data grab is valid

Appendix A: Resolution versus Height Chart

This chart serves as a reference of resolution count with its corresponding height.



Note: Interpolation is applied to resolution count beyond 2 m.

Figure 18. Resolution vs Height Chart

Appendix B: External Illumination Guide

This section provides information and reference schematics in utilizing the LED_N pin from PMW3901MB to support an external LED circuitry. The intent of having an external LED circuitry is to provide the appropriate illumination necessary for user-defined applications. The advantage of syncing the LED_N pulse to drive the external LED is a good power saving feature, especially in wireless and battery-powered applications. While this section aims to provide guidance in utilizing the LED_N pin, user owns the responsibility to select the appropriate LED and design its circuitry to meet the desired end application.

For power saving purposes, LED_N pulsing is not enabled by default. To enable the LED_N pulsing, refer below procedure:

1. Power up PMW3901MB and initialize register settings as outlined in **Section 8.2 Performance Optimization Registers**.
2. Perform below register writes in sequence:

Address	Value
0x7F	0x0E
0x72	0x0F
0x7F	0x00

3. To monitor the LED_N pulsing, connect the LED_N pin to V_{DDIO} via a 1KΩ resistor. By probing the LED_N pin, one can observe the pulses as shown in below image.

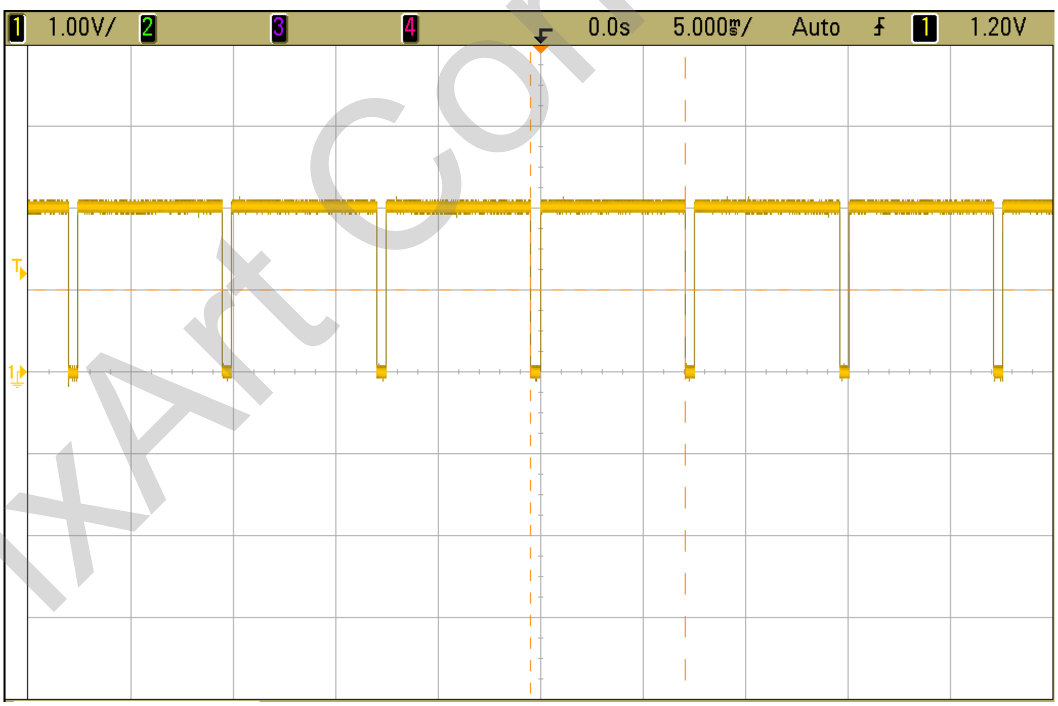
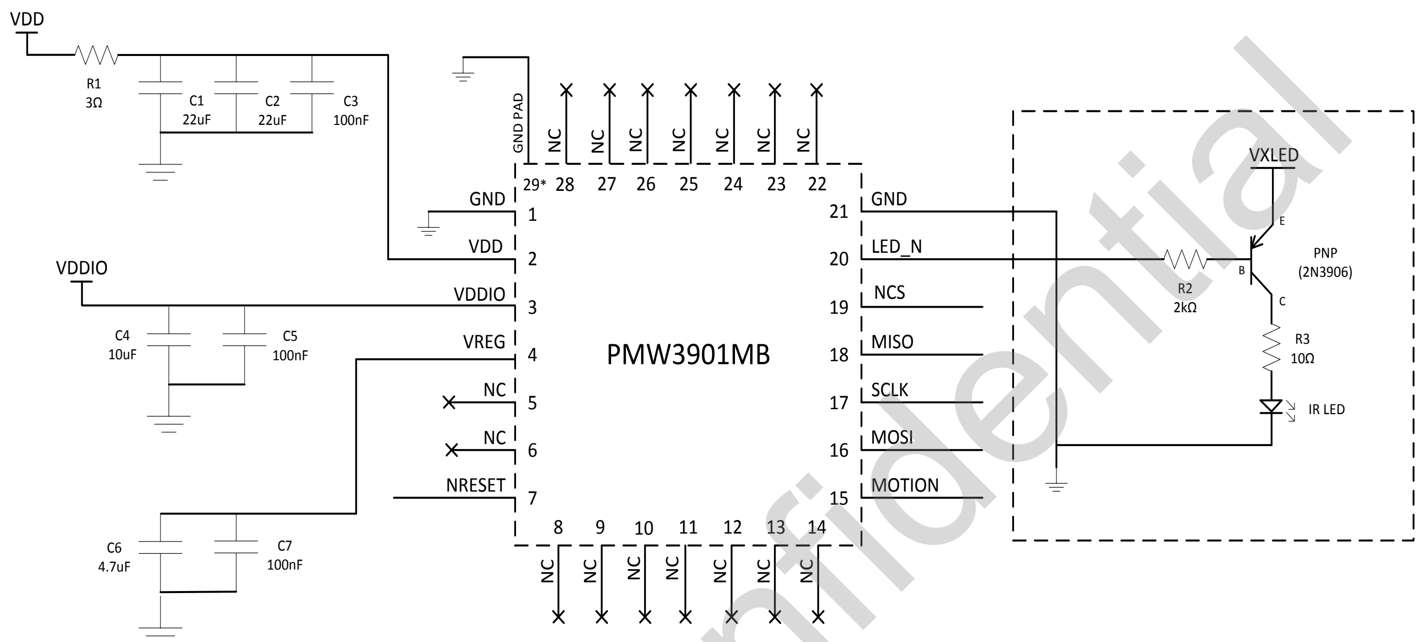


Figure 19. LED_N pulsing

An example of syncing the LED_N pulse to drive an external LED circuitry using an IR LED and a PNP transistor (Part Number: 2N3906) is shown below:



Note:
1. All capacitors must be placed as close as possible to VDD, VDDIO & VREG pins.
2. Ceramic non-polarity capacitors are recommended.

Figure 20. Schematics to drive external LED circuitry

Using the above LED circuitry, the corresponding characteristics of the V_{XLED} and I_{XLED} are shown in below table:

R2 (Ω)	Min V_{XLED} (V)	Max V_{XLED} (V)	Min I_{XLED} (mA)	Max I_{XLED} (mA)
2 k	2.70	3.30	60	70

Revision History

Revision No.	Date Released	Description of Change(s)
V1.10	June/20/2017	Page 7 – Table 1: Change Pin 20 from "NC" to "LED_N". Page 8 – Table 3: Update min lux number. Page 15: Update Figure 8 (Reference Schematics). Page 29: Update Table 10 (Performance Optimization Registers). Page 43: Add Appendix B (External Illumination Guide).